WE CLAIM:

1. A two-chip/single-die packet switch operating in an internal memory mode in storing packet data of a received packet in an internal memory store, and operating in an external memory mode in storing the packet data in an external memory storage connected to the packet switch, the packet switch comprising:

   a. a packet reception block including only internal memory mode logic for storing received the packet data in the internal memory store and for issuing a packet processing job request in respect of the packet stored in the internal memory store;

   b. a packet processing block including only internal memory mode logic for performing operations on packet header information and for issuing a packet transmission job request in respect of the processed packet;

   c. an external memory storage interface including only external memory mode logic, the external memory storage interface being in communication with the external memory storage;

   d. an external memory storage manager block including only external memory mode logic for tracking external memory storage occupancy; and

   e. a packet data transfer engine including both internal and external memory mode logic for conveying the packet data between the internal memory store and the external memory storage interface responsive to the transmission job request.

2. The two-chip/single-die packet switch claimed in claim 1, further comprising an internal memory manager block including internal memory mode logic only for tracking internal memory store occupancy.

3. The two-chip/single-die packet switch claimed in claim 1, wherein the packet data transfer engine further comprises:

a. a queue managed block including internal memory mode logic for processing the packet transmission job request and including external memory mode logic for conveying the packet data between the internal memory store and the external memory storage interface; and

b. a receive adaptation block including internal memory mode logic for reading the packet data from the internal memory store and including external memory mode logic for writing the packet data to the external memory storage interface.

4. The two-chip/single-die packet switch claimed in claim 3, further comprising:

a. an internal memory store interface including only internal memory mode logic providing access to the internal memory store; and

b. the packet data transfer engine further comprising a transmit adaptation block including external memory mode logic for reading the packet data from the external memory storage interface and including internal memory mode logic for writing the packet data to the internal memory store via the internal memory store interface.

5. The two-chip/single-die packet switch claimed in claim 3, further comprising an internal memory store interface including internal memory mode logic for accessing the internal memory store and external memory mode logic for receiving the packet data from the external memory storage interface.

6. The two-chip/single-die packet switch claimed in claim 1, further comprising a packet transmission block including only internal memory mode logic for retrieving the packet data from the internal memory store in transmitting the packet via an output port.

7. The two-chip/single-die packet switch claimed in claim 1, wherein the packet processing block further comprises one of: a search logic for determining an output port for the packet, and a classification logic for classifying the received packet.

8. A method of accessing Double Data Rate Synchronous Dynamic Random Access Memory (DDR SDRAM) memory storage employed in a packet switch, the DDR SDRAM memory having a plurality of memory banks for storing packet data of a plurality of packets, the method comprising steps of:

a. segmenting packet data into variable size burst units;

b. sequencing a plurality of burst unit memory write operations ensuring that each burst unit memory write operation writes packet data to a memory bank different from the previous burst unit memory write operation;

c. sequencing a plurality of burst unit memory read operations ensuring that each bust unit memory read operation reads packet data from a memory bank different from the previous burst unit memory read operation;

d. arranging the plurality of sequenced burst unit memory write operations in a plurality of write windows;

e. arranging the plurality of sequenced bust unit memory read operations in a plurality of read windows; and

f. performing memory access operations interleaving the write windows with the read windows.

9. The method claimed in claim 8, wherein segmenting packet data into variable size burst units, the method further comprises a step of: segmenting packet data in respect of packets received via a plurality of input switch ports prior to storing the packet data into the memory storage.

10. The method claimed in claim 9, further comprising a prior step of: enforcing packet acceptance control.

11. The method claimed in claim 10, wherein enforcing packet acceptance control, the method further comprises a step from: selectively accepting a packet, and selectively discarding another packet.

12. The method claimed in claim 9, wherein sequencing the plurality of memory burst unit memory write operations, the method further comprises a step of: preferentially scheduling write burst units corresponding to a packet from one of: a packet received via a high bandwidth input port, a high quality-of-service packet, a packet of a particular type of service, an alarm packet, and a signaling packet.

13. The method claimed in claim 12, wherein preferentially scheduling write burst units, the method further comprises a step of: delaying scheduling of write burst units totaling less than ten memory access cycles long to a single bank.

14. The method claimed in claim 8, wherein segmenting packet data into variable size burst units, the method further comprises segmenting packet data in respect of packets stored in the memory storage for transmission via a plurality of output switch ports.

15. The method claimed in claim 14, wherein sequencing the plurality of memory burst unit memory read operations, the method further comprises a step of: preferentially scheduling read burst units corresponding to packets from one of: a packet to be transmitted via a high bandwidth output port, a high quality-of-service packet, a packet of a particular type of service, an alarm packet, and a signaling packet.

16. The method claimed in claim 14, wherein sequencing the plurality of memory burst unit memory read operations, the method further comprises a step of: delaying scheduling of read burst units corresponding to packets destined to a congested output port.

17. The method claimed in claim 14, wherein sequencing the plurality of memory burst unit memory read operations, the method further comprises a step of: delaying scheduling of read burst units totaling less than ten memory access cycles long to a single bank.

18. The method claimed in claim 8, wherein segmenting packet data, the method further comprises a step of: segmenting packet data into at least four memory access cycles long burst units.

19. The method claimed in claim 18, wherein segmenting packet data, the method further comprises a step of: segmenting packet data into burst units transferring at least 49 bytes of packet data.

20. The method claimed in claim 8, further employing windows at least 128 memory access cycles long.